

Appl. No.: 10/732,962
Attr. Dckt.: MIO0088V3/40509.280

Amendments to the Claims

1. (Currently Amended) A semiconductor assembly comprising:
 - a nitridation receptive material;
 - a nitridation resistive material having an unmodified surface; and
 - a silicon dioxide monolayer formed directly on said nitridation receptive material and said unmodified surface of said nitridation resistive material.
2. (Original) The semiconductor assembly as recited in claim 1, further comprising a nitride film provided over said monolayer.
3. (Original) The semiconductor assembly as recited in claim 1 wherein said nitridation receptive material is selected from the group consisting of polysilicon and hemispherical-grained (HSG) silicon.
4. (Original) The semiconductor assembly as recited in claim 1 wherein said nitridation resistive material is an insulative material selected from the group consisting of BoroPhosphoSilicate Glass (BPSG) and oxides.
- 5-23. (Cancel)
24. (Currently Amended) A floating gate dielectric provided on a semiconductor substrate comprising:
 - a nitridation receptive material and a nitridation resistive material having an unmodified surface;
 - a conformal silicon dioxide monolayer provided to said nitridation receptive material and said unmodified surface of said nitridation resistive material via chemisorption; and
 - a uniformly thick dielectric compound on said monolayer.

Appln. No.: 10/732,962
Attrtry Dekt.: MIO0088V3/40509.280

25. (Original) The floating gate dielectric as recited in claim 24, wherein said dielectric comprises a material selected from silicon nitride and tantalum oxide.
26. (Original) The floating gate dielectric as recited in claim 24, wherein said monolayer comprises a material selected from silicon dioxide and tantalum.
27. (New) The semiconductor assembly as recited in claim 1, further comprising a silicon nitride layer provided on said silicon dioxide monolayer.
28. (New) The semiconductor assembly as recited in claim 1, wherein said assembly forms part of a storage capacitor.
29. (New) The semiconductor assembly as recited in claim 1, further comprising a silicon nitride layer provided on said silicon dioxide monolayer, wherein said silicon nitride layer is oxidized.
30. (New) The semiconductor assembly as recited in claim 1, further comprising a silicon nitride layer provided on said silicon dioxide monolayer, wherein said silicon nitride layer and said silicon dioxide monolayer have a combined thickness 50Å or less.
31. (New) The semiconductor assembly as recited in claim 1, wherein said silicon dioxide monolayer has a thickness about 2Å or less.
32. (New) The semiconductor assembly as recited in claim 1, further comprising a nitride layer provided on said silicon dioxide monolayer, wherein said silicon dioxide monolayer and said nitride layer were provided insitu.

Appl. No.: 10/732,962

Attr. Dckt.: MIO0088V3/40509.280

33. (New) The semiconductor assembly as recited in claim 1, wherein said nitridation resistive material forms a conductive bottom plate.

34. (New) The semiconductor assembly as recited in claim 1, wherein said dielectric film layer comprises a material selected from silicon nitride and tantalum oxide.

35. (New) The semiconductor assembly as recited in claim 1, wherein said nucleation monolayer comprises a single atomic layer of a material selected from silicon dioxide and tantalum.

36. (New) The semiconductor assembly as recited in claim 1, wherein said nonconductive nucleation monolayer and said dielectric layer were provided insitu.